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Ivan S. Kavrukov, Esq.
Cooper & Dunham LLP
1185 Avenue of the Americas
New York, NY 10036

EXAMINER	
WOODS, ERIC V	

ART UNIT	PAPER NUMBER
2672	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,111	ISHIHARA, HIROSHI	
	Examiner	Art Unit	
	Eric V. Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 1-7, filed 28 April 2005, with respect to the rejections under 35 U.S.C. 112, first and second paragraphs have been fully considered and are persuasive in certain regards in view of applicant's amendments. The rejection of certain claims under 35 U.S.C. 112, first and second paragraph, has been withdrawn. Specifically, all 112 rejections specifically dealing with the word 'overlap' have been withdrawn.

2. All claim objections stand withdrawn, as applicant has corrected the cited deficiencies via amendment.

3. As for objections to the specification and drawing, see those sections below for a listing of the objections that have not yet been corrected.

4. As for the remaining rejections under 35 U.S.C. 112, see that section below for a listing of the rejections retained.

5. Briefly, applicant uses means plus function language in the claims but then refuses to correct the drawings and specification to reflect precisely what structures and functions are required to fulfill those limitations in the claims. Applicant further states that the presumptive connection method, e.g. a bus, is not in the specification or claims, which leads to dual questions concerning enablement and new matter. Applicant is required to address both of those issues in reply to this Office Action, e.g. to specifically point out how the present invention meets the enablement requirement or to remove the 'means plus function' language, and to point out how any material added in response

has antecedent basis and should be entered, since applicant has freely admitted in Remarks page 2 that there is no intended structural limitations, but applicant still insists on using means language under 35 U.S.C. 112, sixth paragraph.

6. Applicant's arguments, see pages 3-7 of Remarks filed 28 April 2005, with respect to the rejection(s) of claim(s) 1-54 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made as set forth below.

7. Applicant further asserts in Remarks page 1 that one of ordinary skill in the art would be knowledgeable that a "run aggregate figure" was a well-known part of run-length encoding (RLE). Examiner disputes this assertion. One of ordinary skill in the art of computer graphics would not necessarily be aware of all of the intricacies of RLE and other techniques used in printer or PDL processing that commercial printers utilize. If applicant intends to hold this position, applicant needs to submit documentation of some sort (preferably, a reference paper or copies of relevant chapters of a textbook) to prove this point and to provide justification for this assertion.

Specification

8. The disclosure is objected to under 35 U.S.C. 112, first paragraph, as being non-enabling. There are several terms used in the specification, all of which involve "aggregate", e.g. "run aggregate figure", "run aggregate data", etc., none of which are clearly defined at any given point. Consequently, one of ordinary skill in the art would not know how to make and/or use the invention.

9. The specification is objected to because the bus element shown in Fig. 1 is not mentioned in the drawing or the specification, and so represents an omission of an essential element. Also, the connections between the bus element and the other elements are not made clear in either the drawings or the specification – that is, whether the connections are through the bus or not, or bypass it.

10. The arguments put forth in the response to the first Office Action were not found to be persuasive with respect to the drawings and specification. Applicant is warned and put on notice that a continued refusal to correct these deficiencies will result in the next response by applicant being held non-responsive.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

11. The drawings are objected to because the (presumed) bus element in Figs. 1 and 2 is not labeled. There is obviously a bus or communications device that the CPU element is connected to; this element is an essential element to understanding the functioning of the device, and so must be labeled. Also, it is not clear whether the "graphic overlay detection unit" 11 and the "immediately preceding graphic data memory" 21 are both connected to the bus, to each other, or both. Also, it is not clear whether connections between elements 20 and 11 and element 12 and 23 are through

the bus or not, as the connection between elements 10 and 20 is clearly not through the bus and is shown passing through it, whereas in the other drawings it is not.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

12. The arguments put forth in the response to the first Office Action were not found to be persuasive with respect to the drawings and specification. Applicant is warned and put on notice that a continued refusal to correct these deficiencies will result in the next response by applicant being held non-responsive.

Claim Rejections - 35 USC § 112

13. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

14. Claims 4-7, 13-16, 22-25, 31-34, 40-43, and 49-52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to

enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. That is, the term "run aggregate figure" is not clearly defined anywhere in the specification, and has no art-accepted meaning. As such, the disclosure is not enabling and thus neither is any claims that incorporate this term.

15. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.**

16. Claims 4-7, 13-16, 22-25, 31-34, 40-43, and 49-52 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

17. Claims 4-7, 13-16, 22-25, 31-34, 40-43, and 49-52 are rejected as being indefinite for failing to define "run aggregate figure." As such, the subject matter being claimed is not clear.

18. Claims 1-8 and 29-54 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the communications device between various components, principally the memories and the CPU as shown in Figs. 1 and 2, which are the embodiments of the recited 'means' and they very clearly show such components.

19. Applicant admits in Remarks page 2 that a 'bus' is never mentioned in the specification and/or claims. However, the problem with that argument is that applicant continues to recite 'means' in all of the above-cited claims. When means plus function

language is used, the structural limitations from the specification and drawings are necessarily included in any analysis of those claims. As such, the "overlay detection means" recited in all the independent claims clearly performs such overlay detection, and that requires the components of Fig. 1 and 2 to be connected in some fashion, and the use of 'means' also requires that the other structural components be connected to the overlay detecting means in the specified manner. Again, applicant has not clarified this point – as such, rejections and objections are being held against all applicable claims.

20. Finally, very clearly there are two components of the recited 'overlay detecting means' – which is element 3 in Figs. 1 and 2, and those are connected in some fashion as shown in Figs. 1 and 2.

Applicant is put on notice and warned that Failure to address these rejections under 35 U.S.C. 112 in the response to this Office Action **will** result in the response being held **Non-Responsive**.

**Please note: examiner is interpreting the term "run aggregate figure" as used in the claims in light of the specification and Figs. 6A-6C; that is, since applicant describes printing and page description languages, the term "run aggregate figure" is taken to mean blocks of text, characters, images, or similar.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

> invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. Claims 1, 3-10, 12-19, 21-28, 30-37, 39-46, and 48-54 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Venable in view of Duluk and Murakami et al (US 6,148,118).

[Claim 10 [and all subsequent claims, e.g. 10-54 having the words "means" in them] is a substantial duplicate of claim 1, the only difference being that the word 'means' is added one time. The means in question – overlay detecting means – is that specified by Venable. Reference Venable teaches the use of rectangles to detect overlap, as shown in Fig. 14. Further, Venable teaches the use of bounding rectangles to enclose other polygons in Fig. 13 and 0088, which would *prima facie* enclose text and similar and teaches processing of rectangular figures in 0073, and further states that the methods can be applied to polygons having any other shape, including circular or elliptical ones, which would most certainly encompass the "run aggregate figures" of applicant. The "run aggregate figures" shown in applicant's Figs. 6A-6C would be equivalent to lines of text that are encapsulated by bounding boxes and then processed together. As such, any means for detected overlap of rectangular features would *prima*

facie be effective for analyzing stacks of rectangular figures. The "means" recited by applicant would correspond to the rectangular overlap detection method shown in Venable Fig. 14 (comparable to applicant's Figs. 5A-5C, for example). Thusly, the overlay detecting means taught by Venable corresponds with that of the applicant.]

[Further, for all claims that are dependent on claim 10 (e.g. 11-18) please note that the above discussion on 'means' applies to those claims as well, so that limitation will not be addressed, as those claims are all exact duplicates of those of claims 1-9.]

[Claim 19 is a duplicate of claim 1 with the word "method" substituted for apparatus. Claim 28 is a duplicate of claim 1 with the word "printing" substituted for "image processing." Claim 37 is a duplicate of claim 1 with the words "host PC" substituted for "image processing apparatus." Claim 46 is a duplicate of claim 1 with the word "forming" substituted for "processing". These substitutions do NOT change the scope of the claims and so the same rejections that are valid on claim 1 and the dependent claims therein are equally valid, with no further comment, on these claims. Finally, Venable 0026 shows a printing system (applicant's claim 28), Venable (see Venable claims 1-8) claims a method (applicant's claim 19), and Venable 0060 and 0057 teach that a general purpose computer can be an image input device and the device shown has a general purpose computer or data processing unit on it [so it would be obvious that, under certain circumstances, these elements could be combined; a general purpose computer would also be an image forming apparatus] (applicant's claim 37 and 46).]

24. As to claims 1, 10, 19, 28, 37, and 46,

An image processing apparatus which sequentially processes graphic rendering instructions for image data, said graphic rendering instructions including first and second graphic rendering instructions, said first graphic rendering instruction being input immediately preceding said second graphic rendering instruction, said first graphic rendering instruction containing first rendering data representing a first original image to render a first output image, said second graphic rendering instruction containing second rendering data representing a second original image to render a second output image, said first original image being overlaid by said second original image, said image processing apparatus comprising: (Venable 0012-0017, that is, referring to the method claim; 0049, definition of an item of data, which clearly meets the recited "containing first rendering data representing a first original image", 0052 and 0056 for more definitions, e.g. definition of image processing and of a version of an image, which is defined to be a second image produced using an item of data of the first image processed in some way. Further, in 0060-0061 it is disclosed that a printer may contain all the components shown in Fig. 2, which roughly correspond to applicant's Fig. 1, insofar as it contains memory and a CPU as claimed by applicant. Further, as applicant discusses in the specification, 0005 and 0061 disclose that objects and data to be rendered can be text, images, graphics, structured image documents, and files with multiple layers, e.g. 0062 – it can be a page description language.)(Duluk discloses sequential processing of primitive groups in Fig. 15 for the shown pipeline – see 25:45-55, 26:14-20. Further, as illustrated in Fig. 24, images are processed as they overlap. Duluk specifically teaches this limitation in the context of clipping images, e.g. where an object overlaps another

one, it very clearly will clip the portion of the images not in the view volume, and then will perform hidden surface removal, which clearly functions by eliminating polygons that are occluded by others at a more shallow depth (16:56-17:35). Further, dynamic microcode generation is performed where the data and instructions are both fed into the pipeline sequentially 38:15-55.)

Overlay detector configured to perform an overlay detection to detect an overlay of the first and second original images which are rendered based on the first and second rendering data by the first and second rendering instructions, respectively; and (Venable Fig. 14, processes disclosed in 0015 and 0021, would be rendered as disclosed in 0005 and 0061. These processes would inherently require an "overlay detector" as recited by applicant; anything that performs overlap detection fulfills this requirement. Further, Fig. 5 illustrates how 'background' and 'foreground' regions are identified, where these are the areas from the first and second images respectively. Turning to Duluk, obviously overlap detection is done on a per-fragment basis for rendering.)

A memory storing the first rendering data contained in the first graphic rendering instruction, wherein the overlay detector specifies a portion of the first original image to be overlaid by the second original image upon detecting an overlay of the first and second original images, deletes a specified portion and draws a third output image, based on the original images, in which the specified portion of the first original image is deleted and stores the second graphic rendering data into the memory (Venable Fig. 2 shows a general category block labeled 'memory' that contains both ROM and RAM

which meets the recited 'memory'. As shown in Venable Fig. 5, the 'non-imagery' regions are eliminated (step 126), which corresponds to the "specified portion" recited by applicant above. Furthermore, as shown in Fig. 12, a bounding rectangle is formed around polygons and items for overlap analysis. Turning back to 0015-0018, very clearly the first two images are input and the third image is output with the 'specified region' removed. Given that the memory shown in Fig. 2 is the only memory shown, it is inherent in the operation of a digital computer (CPU) that it requires memory, and thus would use the memory shown, thus fulfilling the recited limitations of claim 1. Further, all such images would be loaded into this memory for processing. Also, see 0005 and 0061 for rendering limitation. Images are stored in the memory in 0060-0061. Turning now to Duluk, several memories are shown in Fig. 15, and the sort memory uses paging techniques (26:15-21). The 'intermediate memory' shown in applicant's Fig. 1 embodiment would correspond to the frame buffer (element 17000) in Fig. 15, or various other memory elements shown. Further, fragments are stored after compositing and overlap / hidden surface removal in the frame buffer of Duluk before they are displayed or written to the output device.)

Murakami is brought in to cover the final details. Applicant clearly argues that the combination of Venable with Duluk would not, per se, delete the overlapping portion of the first image. Examiner concedes that Venable teaches image blending. However, it is well known in the art that deleting the overlapping portion of one of the overlapping image would save memory.

Clearly, this concept is well known in the art (see for example Akasawa et al (US 6,867,801). Akasawa teaches a digital camera which is used to generate panoramic images, e.g. images that overlap with each other. For example, in Figs. 9A-9D the overlap is sensed and the overlapping portions of the first and second images are identified. Further, in Figs. 20A-20D the full process is shown wherein the overlapping portions identified in Figs. 9A-9D for example are deleted and the final image is created with the erased portions of the second and subsequent images that overlap (see for example 14:10-15:25).

US 6,148,118 (23:5-23:23) to Murakami et al teaches that the overlapping portion of various images are deleted. Murakami teaches a method for combining images to allow large documents to be copied, e.g. a document can be scanned in multiple portions and the images combined. The overlapping areas are deleted (23:5-23:23), with emphasis on the process in 6:20-7:2. Namely, the images are stored in image memory A and B and then combined to be output to memory C. Specifically, see Fig. 4, where the overall process flow is shown. The key to this particular combination is found in 6:63-67, where image memory C may store data **equal to or smaller than** A3. Clearly, this means that data is removed during the joining process, and as stated in 23:5-23:23 such overlap can simply be deleted to save memory, as is suggested in 6:20-7:2.

Reference Venable discloses all the limitations of the claim except explicitly specifying sequential processing of images and the storing of the third image to memory. Reference Duluk teaches sequential processing of instructions containing

image data and rendering instructions, particularly in 38:15-55, where dynamic microcode generation for each fragment is disclosed (e.g. instructions for processing each fragment are sent along with each fragment, thus forming the first and second graphic rendering instructions and rendering data claimed by applicant). Also, It would have been obvious (because the technique is well-known in the art) to one having ordinary skill in the art at the time the invention was made to process instructions sequentially, as conventional rendering apparatuses process instructions in this manner. Further, it is well known in the art to store the results of image processing in some kind of memory before they are output (e.g. a frame buffer – see Duluk). Duluk establishes sending rendering data into the pipeline with instructions in the discussion on dynamic microcode generation. Reference Venable teaches in 0063 that images are stored in a frame buffer, so it would be *prima facie* obvious to store the third image there. Finally, it would have been obvious to one of ordinary skill in the art to put the second instruction (or image or data) into the system (rendering engine, interpreter, entity, etc.) immediately after the first instruction, as they would be processed together (see Duluk for notes on how vertices are fed into the pipeline in the Background and Generic Pipeline sections).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the overlap removal techniques of Venable and the rendering techniques of Duluk, since the techniques of Duluk (3:10-16, 5:39-60, 6:30-65, as applied to OpenGL standard, which handles both 2D and 3D applications – see Venable 0005 where it is taught that images are rasterized for rendering processing and

Duluk 1:18-50 as well) are taught to speed up conventional rendering processes like those used in Venable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Venable and Duluk with Murakami since Murakami clearly teaches methods for combining images that take up less memory, which is the goal stated by applicant, and further Murakami is directed to the same problem solving area as Venable, that is image reproduction on copiers, and the addition of Murakami to Venable would allow Venable to more easily handle large images and use less memory in the combination process. The combination is not improper hindsight because Murakami provides the motivation. Further, Murakami is merely added to prove that it is well known and obvious in the art to delete the overlapping portion, where the blending solution of Venable is chosen as slightly more optimal in certain circumstances depending on the document and/or graphics involved in the overlapped region, but with the addition of Murakami, the user could choose which mode – blending or deletion was preferred, particularly in situations where memory constraints were involved.

25. As to claims 3, 12, 21, 30, 39, and 48,

The image processing apparatus as defined in claim 1, wherein said graphic rendering instructions are configured to be converted into at least one of intermediate data represented by coordinate information and a PDL language. (Reference Venable teaches the use of a PDL as output from the processing performed in 0062, which fulfills all the recited limitations of the claim. Since only the primary reference is utilized, no separate combination or motivation is required (which fulfills the "at least one of"

limitation recited above. The motivation and combination of the rejection for the parent claim is herein incorporated by reference.)

26. As to claims 4, 13, 22, 31, 40, and 49,

The image processing apparatus as defined in claim 1, wherein each of the first and second original images is configured to include at least one of rectangle figure and run aggregate figure. (Reference Venable teaches in Fig. 14 the use of bounded rectangular regions for image processing as claimed by applicant. Further, since Venable teaches in 0026 that Fig. 1 is an embodiment of a printing system, it would be *prima facie* obvious that input data from a scanner (Fig. 3) or printer as taught by Venable would contain words, text, and images, of which at least the text would be rectangular and thus meet the "run aggregate figure" limitation. Venable teaches the use of rectangles in 0010, and the use of known prepress techniques in 0011, which include PDLs as disclosed in 0061, so PDLs could be used as the input as well. Further, since images are scanned based on a pixel-by-pixel basis, there would be rectangular elements in any first or second image. The platen of the scanner shown in Fig. 3 is rectangular anyway, so the outer perimeter would be rectangular *prima facie*. Finally, in 0073, Venable specifically states that "rectangular figures will be treated", thus meeting this recited limitation. Since only the primary reference is used, no separate motivation or combination is required. The motivation and combination of the rejection for the parent claim is herein incorporated by reference.)

27. As to claims 5, 14, 23, 32, 41, and 50,

The image processing apparatus as defined in claim 4, wherein the overlay detector is configured to perform the overlay detection by each run when the overlay detection means detects an overlay of the run aggregate figures.

(Reference Venable teaches the use of rectangles to detect overlap, as shown in Fig. 14. Further, Venable teaches the use of bounding rectangles to enclose other polygons in Fig. 13 and 0088, which would *prima facie* enclose text and similar and teaches processing of rectangular figures in 0073, and further states that the methods can be applied to polygons having any other shape, including circular or elliptical ones, which would most certainly encompass the "run aggregate figures" of applicant. The "run aggregate figures" shown in applicant's Figs. 6A-6C would be equivalent to lines of text that are encapsulated by bounding boxes and then processed together. As such, any means for detected overlap of rectangular features would *prima facie* be effective for analyzing stacks of rectangular figures. The "means" recited by applicant would correspond to the rectangular overlap detection method shown in Venable Fig. 14 (comparable to applicant's Figs. 5A-5C, for example). Since only the primary reference is used, no separate motivation or combination is required. The motivation and combination of the rejection for the parent claim is herein incorporated by reference.)

28. As to claims 6, 15, 24, 33, 42, and 51,

The image processing apparatus as defined in claim 4, wherein when the overlay detector is configured to detect an overly of the run aggregate figures, the overlay detecting means is configured to generate a circumscribing rectangle for the run aggregate figure of the first and second original images and, after the overlay detecting

means detects an overlay between the circumscribing rectangle for the run aggregate figure for the first and second original images, to determine the run aggregate figure included in the run aggregate figure of an overlaid portion between the first and second original images of the circumscribed rectangle.

[The overlay detector would *prima facie* be capable of detecting overlap between the "run aggregate figures," regardless if it were so configured according to applicant's specification (see 112 1st objection above).] Reference Venable teaches the use of rectangles to detect overlap, as shown in Fig. 14. Further, Venable teaches the use of bounding rectangles to enclose other polygons in Fig. 13 and 0088, which would *prima facie* enclose text and similar and teaches processing of rectangular figures in 0073, and further states that the methods can be applied to polygons having any other shape, including circular or elliptical ones, which would most certainly encompass the "run aggregate figures" of applicant. The "run aggregate figures" shown in applicant's Figs. 6A-6C would be equivalent to lines of text that are encapsulated by bounding boxes and then processed together. As such, any means for detected overlap of rectangular features would *prima facie* be effective for analyzing stacks of rectangular figures. The "means" recited by applicant would correspond to the rectangular overlap detection method shown in Venable Fig. 14 (comparable to applicant's Figs. 5A-5C, for example). Since only the primary reference is used, no separate motivation or combination is required. The motivation and combination of the rejection for the parent claim is herein incorporated by reference.

29. As to claims 7, 16, 25, 34, 43, and 52,

The image processing apparatus as defined in claim 6, wherein the overlay detector is configured to determine whether, for the run aggregate figure included in the run aggregate figure of an overlaid portion between the first and second original images of the circumscribed rectangle, to perform the overlay detection by each run.

Reference Venable does not explicitly teach the configurability of the overlap detection means to choose whether or not to perform overlay detection. It would be obvious to one of ordinary skill in the art to check whether a rectangle or primitive element overlapped before performing the actual overlap detection on two specific polygons or rectangles. Reference Duluk teaches the inclusion of dynamic microcode with data instructions for rendering processing, which would allow for the configurability of elements within the graphics engine. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the overlap detection of Venable with the rendering of Duluk, since the techniques of Duluk (3:10-16, 5:39-60, 6:30-65, as applied to OpenGL standard, which handles both 2D and 3D applications – see Venable 0005 where it is taught that images are rasterized for rendering processing and Duluk 1:18-50 as well) are taught to speed up conventional rendering processes like those used in Venable.

30. As to claims 8, 17, 26, 35, 44, and 53,

The image processing apparatus as defined in claim 1, wherein the second output image is configured to be overwritten on the third output image.

Venable teaches in 0015-0018 very clearly that the first two images are input and the third image is output with the 'specified region' removed. Further, it is well known in

the art to store the results of image processing in some kind of memory before they are output. Reference Venable teaches in 0063 that images are stored in a frame buffer, so it would be *prima facie* obvious to store the third image there. It would be obvious to one of ordinary skill in the art to allow the second image to be overwritten (e.g. if as in the case of Fig. 3, the second image were of background against which an object was placed and it was desired to only capture the object and then combine it with the first image). Reference Duluk teaches the inclusion of dynamic microcode with data instructions for rendering processing, which would allow for the configurability of image elements within the graphics engine, particularly to set one as translucent. Duluk teaches a test for transparency in 8:55-67, which could be applied to set overwriting of a particular image or polygon. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the overlap detection of Venable with the rendering of Duluk, since the techniques of Duluk (3:10-16, 5:39-60, 6:30-65, as applied to OpenGL standard, which handles both 2D and 3D applications – see Venable 0005 where it is taught that images are rasterized for rendering processing and Duluk 1:18-50 as well) are taught to speed up conventional rendering processes like those used in Venable.

31. As to claims 9, 18, 27, 36, 45, and 54,

The image processing apparatus as claimed in claim 8, wherein the first and second output image are configured to be drawn with a rendering process based on at least one of a mono chrome, an RGB video color rendering, and a CMYK paint color rendering.

Venable teaches the use of RGB and similar color spaces (0065). Other color spaces (e.g. CMY, YUV, CMYK) are well known in the art and would be obvious to use. Color printers are known in the art – e.g. it is well known, a fundamental principle in the art – to use CMYK color space. The use of a monochrome color space would be *prima facie* obvious that a copying system (0060, Figs. 1 and 2) is being used, and it is common sense that hard copy (0058) would be black and white (e.g. a book). No separate motivation or combination is required, and that of the rejection of the parent claim is hereby incorporated by reference.

32. Claims 2, 11, 20, 29, 38, and 47 are rejected under 35 U.S.C. 103(a) as unpatentable over Venable in view of Duluk and Murakami as applied to claim 1 [and 10, 19, 28, 37, and 46] above, and further in view of McIntosh (McIntosh, John M. "POSTSCRIPT: A Page Description Language.")

33. As to claims 2, 11, 20, 29, 38, and 47,

The image processing apparatus as defined in claim 1, wherein said graphic rendering instructions are configured to be a page description language and each of said graphic rendering instructions are configured to include a fundamental graphic description instruction which handles characters, graphics and images and a rendering attribute instruction handling colors, clipping area designations and rendering arithmetic methods.

Venable teaches the use of a page description language (PDL) in 0062, but does not teach specifics of the instructions. Reference McIntosh teaches that by definition, a PDL is a programming language that defines images and text in a high-level format; an

example of a PDL is Adobe® Postscript™, which includes its own instructions to handle colors, characters, graphics images, etc (pg. 3). Therefore, the recitation of a PDL limitation by applicant *prima facie* includes "fundamental graphic description instructions" that handle all the various aspects of rendering that are required and includes color (pg. 1). Basically, a PDL includes all the information that applicant recites, and it would be obvious to one of ordinary skill in the art to have a split instruction – e.g. one that that handles rendering and one that does graphical description. Reference Duluk teaches the use of clipping as discussed above (3:45-67), and *prima facie* Postscript handles such operations as well. Further, Duluk teaches the use of dual-based instructions, e.g. a vertex or fragment, and dynamic microcode to accompany it through the pipeline (the primitive, and pipeline state data) that would fulfill this requirement (see claim 1 rejection for references). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the PDL and rendering of Venable and Duluk with the PDL of McIntosh, since McIntosh teaches the details of the PDL that Venable clearly states can be the output of the processing (0062).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V. Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-4:30 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 571-272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Eric Woods

JEFFERY BRIER
PRIMARY EXAMINER

June 14, 2005